F.S.A.I., Vol. 8, Nos. 1–3, pp. 125 – 143, 2002

A New Fuzzy Scheme for Multicast based Shared-Memory Asynchronous Transfer Mode (ATM) Switch

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Abstract: In this paper a new fuzzy scheme for multicast variable bit rate (VBR) bursty traffic in shared memory Asynchronous Transfer Mode (ATM) switch has been proposed. In proposed fuzzy scheme, we have considered two fuzzy variables namely line occupancy and buffer occupancy. By applying fuzzification and defuzzification process, allocation-space for each line queue up-to max-line capacity in shared memory switch is determined. The performance of this scheme has been compared with that of static threshold and dynamic threshold schemes. The results have showed that for proposed fuzzy threshold scheme, average unicast as well as multicast cell delay for a given burst length is minimum under different load conditions. Minimum in delay is a good indication for real-time VBR bursty traffic applications. Yet the scheme has its limitations, which are to be overcome.

Keywords: Buffer allocation, fuzzy system, line occupancy, multicasting, variable bit rate.

1. Introduction

In recent years, large technological progress has occurred both in the field of electronics as well as in the field of optics. This progress will allow the economical development of new communication networks running at very high speeds. An explosion in demand for enterprise–wide connectivity is now taking place and certain to accelerate in coming years. It is becoming increasingly difficult for network managers to maintain cost efficiency and respond fully to customer requirements. No single technology can reserve inter working integration and network simplification issues. It seems certain that Asynchronous Transfer Mode (ATM) will play central strategic role in the network of future.

In the last few years, a large number of switching architectures has been proposed [1], [2], [3], and [4]. All the approaches point to the need of a very high speed hardware switches because of the high transfer rates involved; on the other hand, due to statistical multiplexing, buffering is also required in order to avoid packet loss whenever there are multiple input packets arriving simultaneously on different inputs ports and destined for the same output. Only one packet at a time can be transmitted over an output link, the rest must be temporarily stored in a buffer for later transmission.

The management of multicast traffic in shared memory ATM switches is of particular interest. Multicast mechanisms provide group communications by reducing the amount of duplicate traffic in the network to conserve bandwidth and

switch resources [5], [6], [7], and [8]. Many envisioned applications in ATM Networks are multicast in nature and are expected to generate a significant portion of the total traffic. Examples of such application are broadcast video, video conferencing, multi party telephony and work group applications. While using a shared memory switch, a copy network [9] can also be used for replication of multicast cells, and then the copies of multi-cast cells can be stored in their respective logical queues in a shared memory ATM switch for point-to-point switching.

The proper placement and arrangement of the buffering system have a dramatic impact on the switch performance [10]. Buffer management refers to the discarding policy for the input of cells into the buffers and scheduling policy for the output of cells from the buffers. These functions are a component of the traffic control functions handled by the switch management. Inside the switch fabric, the queue needs to be monitored for signs of congestion to alter the switch management and attempt to control the congestion.

Congestion control is an important phenomenon, because ATM is connection-oriented and supports real-time service [11]. The concept of threshold helps in maintaining a fine balance between the number of cells propagated and the average delay observed by a typical cell in a switch [12-15], and [16]. We have studied and simulated [17], [18], and [19] the effect of various threshold schemes to control congestion for multicast burst traffic in shared memory ATM switch, and proposed a fuzzy scheme for the purpose in this paper. In this scheme line occupancy as well as buffer occupancy are represented by fuzzy sets. The degree of membership, associated with line occupancy and buffer occupancy, for a particular set is read from triangular membership functions.

From these membership values and corresponding look up table values in fuzzy terms can be find out. Then by applying suitable defuzzification methods such as min-max or max-min the percentage allocation space to be offered to the incoming burst of cells is determined.

Section 2 and 3 of this paper describes ATM switching system architecture, and shared memory ATM switch respectively. Section 4 details multicast support for shared memory ATM switch. A section 5 presents various applied threshold schemes. Simulation Process is presented in Section 6. Results and Conclusion appears in Section 7 and 8 respectively.

2. ATM Switching System Architecture

ATM has distinct advantages over other switching architecture because of its switched structure and scalability. In ATM every slice of bandwidth can be used for creating point to point connections. The overall structure of the ATM switch shown in Fig. 1.

The Line Interface (LI) performs optical-electrical signal conversion cell synchronization, header Translation, and insertion and extraction of routing

information. The Call Processor (CP) and the Signaling Processor (SP) are concern with the ATM connection setup and release. The switch module routes cells using routing information of the cells.

In this paper, only transport part of switch is modified for supporting multicast traffic and control part is assumed to have a multicast routing table with the normal Virtual Channel Identifier / Virtual Path Identifier (VCI / VPI) translation table.

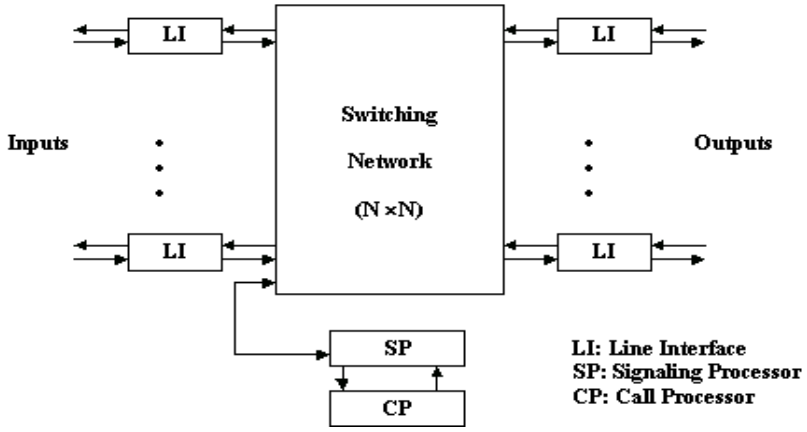

Fig. 1- Overall Structure of ATM Switch

Transport is defined as all physical, means, which are responsible for the correct transportation of the cell from an inlet to an ATM outlet, within the Quality of Services (QoS) of ATM. The control part of the switch is that controls the transport network. It decides which inlet to connect which outlet and accept or discard connection. The decision is based on incoming signaling cell or semi-permanent connection. More details can be found in [9], [20], [21], [22], and [23].

2.1 Switching Network

In an ATM switch, the ATM cells have to be transported from an inlet to one (point-to-point) or more (multicast) outlets. This switching can be combined with concentrator, expansion, multiplexing and demultiplexing of ATM traffic. In switching element there is no co-ordination among arrival cells as far as their destinations request are concerned. Thus more then one cell arriving in the same time slot may be destined to go to the same output port.

This event raises cell conflict so buffering of cells within the switch is provided as shown in Fig. 2.

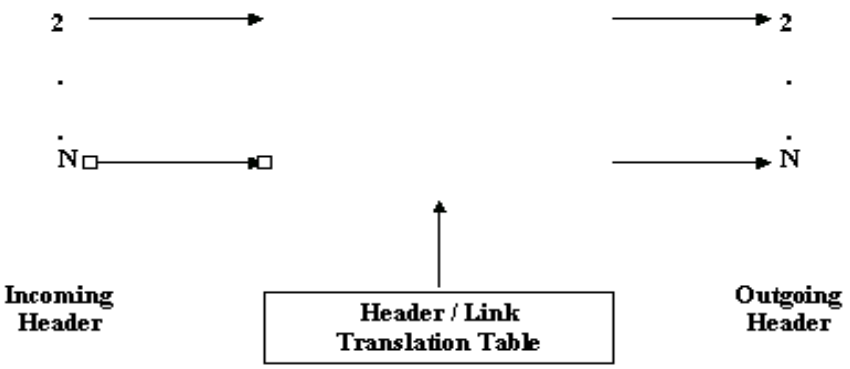

Fig. 2 – Switching Network of ATM Switch

3 Shared Memory ATM Switch

One of the most promising solutions of ATM switches is based on the shared-memory principle. Such switches play a leading role in practical, experimental implementations of ATM. A shared-memory ATM switch provides sharing of memory space among its switches ports and superior cell loss rate performance compared to input-buffer-based and output-buffer-based ATM switches under conditions of identical memory size.

Shared memory ATM switch consists of a single dual-port memory shared by all input and output line as shown in Fig. 3.

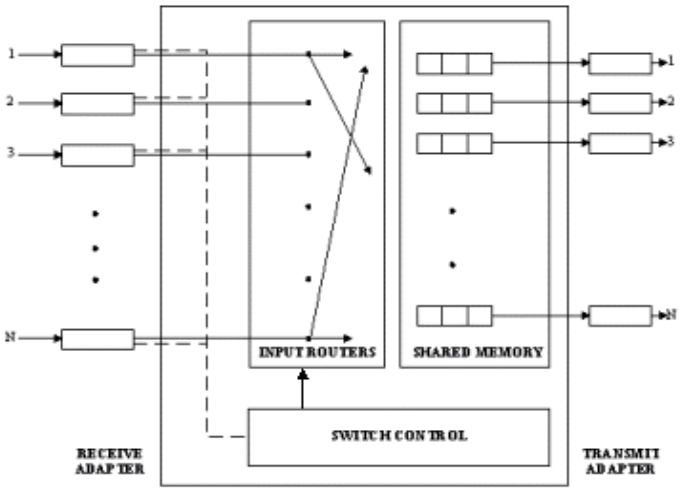

Fig. 3 – Shared Memory Switching Element

Cells arriving on all input lines are multiplexed into a single stream, which is fed to the common storage. Internally to the memory, cells are organised into separate output queues. Simultaneously retrieving packets from the output queues sequentially performs an output stream of cells.

The *N* input ports are connected to the receive adapters and the *N* output ports are connected to the transmit adapters. A 1 to *N* router for each input provides full contention-free connectivity to all output ports. The routing is determined by the destination address in the cell header. Each output is a logical queue with *N* inputs and one output. All output queues are located in a block of shared memory where the space allocated to a specific output varies dynamically with the load of the switch i.e. the memory is full shared among all queues. In-fact switch output queues are implemented through queues of pointers, with each pointer addressing a cell in the shared memory. This allows better memory utilization then fixed memory allocated to each output queue.

For reasons of fairness, the maximum share of memory that can be allocated to each output must be limited to prevent temporarily overloaded connections from using the entire memory space and degrading the throughput of other connection to other outputs. This policy is implemented in the control section of the switch. In shared memory ATM switches two following main constraints must be satisfied.

- The processing time required for determining where to queue up the cells and for issuing the proper signals for the purpose should be sufficiently small to keep up with the flow of incoming cells.
- There is limitation on the memory access speed. Thus the available memory speeds and achievable processing speeds determine the size of the switch.

4. Multicast Support for Shared Memory ATM Switch

Multicast operations are important in supporting point-to-multipoint communications. There are various ways of supporting multicast operation with shared memory architecture. Replication-at-Receiving (RAR) is one of the schemes to support such operation, which has been used for the purpose. In RAR scheme, a multicast cell arriving at the switch and destined to 'm' destinations is first copied 'm' times as represented in Fig. 4.

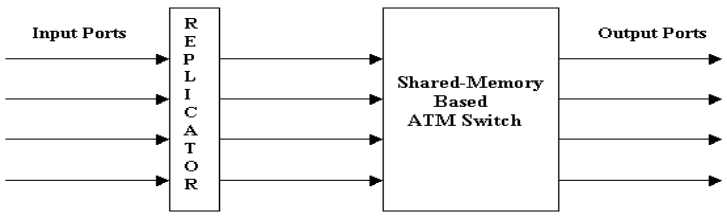

Fig. 4 – RAR Multicast Scheme

A copy of the cell is linked to each output queue to which the multicast cell is destined [24]. All copies are stored in the buffer then each copy is served independently. So this scheme is also known as Multiple Write Multiple Read (MWMR) scheme.

The scheme has been used in several existing shared memory switches because it is relatively simple to implement. While using a shared memory switch, a copy network [9] can also be used for replication of multicast cells, and then the copies of multi-cast cells can be stored in their respective logical queues in a shared memory ATM switch for point-to-point switching. In fact once a cell has been replicated each copy of the cell can be treated in a same way as a uni-cast cell. Consequently, both the control and structure of the linked-lists are basically the same as those used in a uni-cast switch.

The advantage of this scheme is that, this is a straightforward solution to providing multicast support. This scheme is a fair scheme in the sense that copies of a multicast cell destined to a loaded output are more likely to be dropped, and an idle output port would always get its cell if the copies are present in the memory.

4.1 Multicast Traffic Model

Let X be the random variable denoting the number of copies associated with an incoming multicast cell. Let $P(X = r)$ be the probability that the number of copies associated with an incoming multicast cell is r. If f is a fraction of incoming bursts consisting of multicast cells with a geometric fanout, then Effective offered load (E_L):

$$(E_L) = [(1 - f).L] + [f.L.E(X)],$$

while L is the offered load.

If X has a truncated geometric distribution $g(X)$ with the parameter q, then

$$g(k) = P_r[X = k] = \frac{(1-q)q^{k-1}}{1-g_n}, 1 \le k \le n \tag{1}$$

and the average number of copies per multicast cell.

$$E(x) = [\frac{1}{1-q} - \frac{nq^n}{1-q^n}] \tag{2}$$

Thus, the effective offered load (E_L) can be given as follows:

$$E_L = [1-f][\frac{\beta_i}{\alpha_i + \beta_i - \alpha_i\beta_i}] + f[\frac{\beta_i}{\alpha_i + \beta_i - \alpha_i\beta_i}].[\frac{1}{1-q} - \frac{nq^n}{1-q^n}] \tag{3}$$

here α_i and β_i characterizes the duration of the active and idles periods respectively, and *n* is the switch size.

5 Various Applied Threshold Schemes

Most of the ATM switch architectures that have been proposed in the literature use some buffering to accommodate packets whose service has been delayed due to contention for some resource within the switch. The location of these buffers and the threshold scheme directly affect the performance of such a switch. Various threshold schemes, which are applied to control congestion in multicast bursty traffic in shared memory ATM switch are Static Threshold (ST), and Dynamic Threshold (DT) Schemes. The maximum or minimum amount of buffering that should be available to any individual queue, called Static Threshold (ST). In this method [14], an arriving cell is admitted only if the queue length at its destination output port is smaller than a given threshold.

Dynamic Threshold is a scheme to fairly regulate the sharing of memory among different output queue for traffic of a single loss priority. This scheme is conceptually similar to bandwidth balancing in Distribution Queue Dual Bus (DQDB) network and to bottleneck flow control [25]. The DT scheme deliberately wastes a small amount of buffer space, but attempt to equally share the remaining buffer space among the active output queues.

Each output queue attempts to limit its length to some function f of the unused buffer space; output queues with less demand than this can have all the space they wish [14]. At time t, let $T(t)$ be the control threshold and let $Q^i(t)$ be the length of queue i. Let $Q(t)$ be the sum of all of queue lengths, i.e., the total occupancy of the shared memory. If B is the total buffer space, then:

$$T(t) = f(B - Q(t)) = f(B - \sum_i Q^i(t)) \tag{4}$$

An arriving cell for queue i will be blocked at time t if $Q^i(t) \geq T(t)$. All cells going to this queue will be blocked until the queue length drains below the control threshold and/or the threshold rises above the queue length. The simplest method is to set the control threshold to a multiple α of the unused buffer space.

$$T(t) = \alpha.(B - Q(t)) = \alpha.(B - \sum_i Q^i(t)) \tag{5}$$

If α is a power of two (either positive or negative), then the threshold computation is extremely easy to implement.

5.1 Proposed Fuzzy Threshold (FT) Scheme

In ATM shared memory switch, it has the total buffer space B. This buffer space is divided into the number of output line. We use 64 × 64 ATM switch, i.e. buffer space distributed 64 line space. It is to be calculated buffer line occupancies and total buffer occupancy. A binary threshold is considered in each line space. This binary threshold divides the line space into two parts. Below or equal to the threshold level, every arriving cell is given entry to the ATM switch, threshold levels in each line will be change upto maximum line capacity. If total arriving cells in each line is large to maximum line capacity then cells will be lost.

In proposed Fuzzy Threshold Scheme, wherein line occupancy as well as buffer occupancy are represented by fuzzy sets, and these are represented by triangular functions as shown in Fig. 5(a) and 5(b).

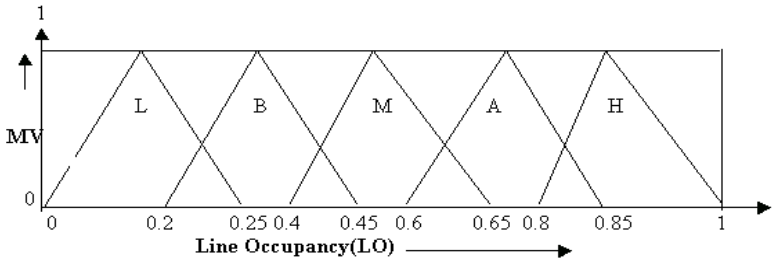

Fig. 5(a) - Triangular Functions for Line Occupancy

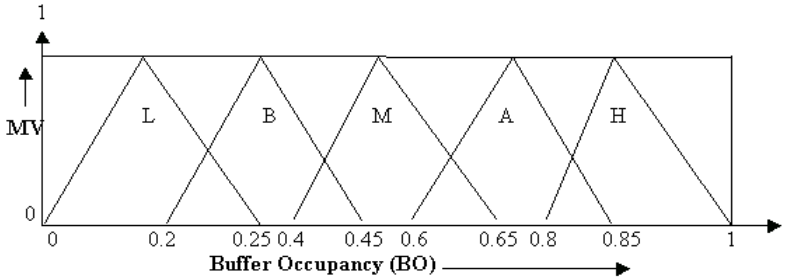

Fig. 5(b) - Triangular Functions for Buffer Occupancy

In the figures *L*, *B*, *M*, *A* and *H* represent Low, Below medium, Medium, Above medium and High membership sets respectively, M.V. represents membership value. From these, the degree of membership, to particular set, associated with each valid buffer occupancy and line occupancy, can be read. This quantification of membership is called fuzzification.

From these membership values and corresponding sets allocating space to be offered again in fuzzy term can be find out. This process is called rule-based inference. As an example, a typical rule is when line occupancy is high and buffer

occupancy is high, threshold value is high, i.e., allocation space will be high as shown in Lookup Table 1(a), and (b).

Then, by applying suitable defuzzification method, such as min-max or max-min defuzzification, the percentage allocation space to offered at that particular line occupancy and at given buffer occupancy is determined. For defuzzification, with the set such as shown in the following Table-2 weighted average is used.

For example, it is assumed that line occupancy as well as the buffer occupancy both are characterized by the fuzzy sets. Assume maximum line capacity is kept at 40 and total buffer space is assumed 200. Suppose, at the time of a new arriving cells at particular queue of buffer, line occupancy = 20 and buffer occupancy =48. When normalized with respect to maximum value, these variables are mapped as line occupancy = 0.5 and buffer occupancy = 0.24. Using Fig. 5(a), and 5(b) for fuzzification it is seen that line occupancy is a member of set *M* with associated value 0.8. Buffer occupancy of set *B* with associated value 0.32 and a member of set *L* with associate value 0.08.

Table 1(a)

Lookup Table - Space Allocated

BO / LO	**L**	**B**	**M**	**A**	**H**
L	L	L	L	B	M
B	L	B	B	M	M
M	B	M	M	A	A
A	M	A	A	A	H
H	A	A	H	H	H

Table 1(b)

Lookup Table - Space Allocated

BO / LO	**L**	**B**	**M**	**A**	**H**
L	L	L	B	B	B
B	B	B	B	M	M
M	M	M	M	A	A
A	M	M	A	A	H
H	A	A	H	H	H

Using Lookup Table 1(a) and min-max method of evaluation, we get the followings:

Line occupancy *M*(0.8) and buffer occupancy *B*(0.32) => Allocated value for threshold *M*(0.32).

Line occupancy *M*(0.8) and buffer occupancy *L*(0.08) => Allocated value for threshold *B*(0.08).

Thus, taking maximum of the two values associated with same membership of set, allocating value for threshold has membership of set *M* with value 0.32 and

membership of set *B* with value 0.08 using the set with weighted average of membership values. Percentage of allocated value for each line in ATM switch for defuzzification, set I of Table 2 is used.

Table 2

Defuzzification Table - L: Low Set, B: Below Medium Set, M: Medium Set, A: Above Medium Set, H: High Set

Set	L	B	M	A	H
I	0.2	0.4	0.6	0.8	1
II	0.4	0.5	0.7	0.9	1
III	0.5	0.6	0.8	0.9	1
IV	0.3	0.7	0.8	0.9	1

Allocated Space (in %) $= [(0.32 * 0.6) + (0.08 * 0.4)]/(0.32 + 0.08) = 0.56\%$ and we multiply with maximum value of line capacity and calculate the threshold level $0.56 \times 40 = 22.4$ (i.e. 22), where 40 is the maximum line capacity of each queue. This fuzzy scheme is applied for total number of line *N* where we used $N \times N$ ATM shared memory switch.

6 Simulation Process

For ATM multicast, the parameters of interest are queuing delay, throughput and cell loss ratio. If there is no multicasting, all the cells are switched to the buffer corresponding to their destination field. But in multicasting case, one cell may be duplicated (not necessarily) and therefore can occupy more than one buffer space. The general simulation process for multicasting in ATM switching can be described as below and represented in the form of flow-chart in Fig. 6.

6.1 Generate Input

The first step is to generate the traffic for the switch and generate the output ports for the cells randomly. Cells are marked either unicast or multicast type according to combination required.

6.2 Setup Load and Buffer

The performance analysis is to be done with varying loads and multicast combinations. Varying OFF periods of the traffic varies load. The buffer size can be varied for performance but in this case, it is taken as 2048 cells space for the switch.

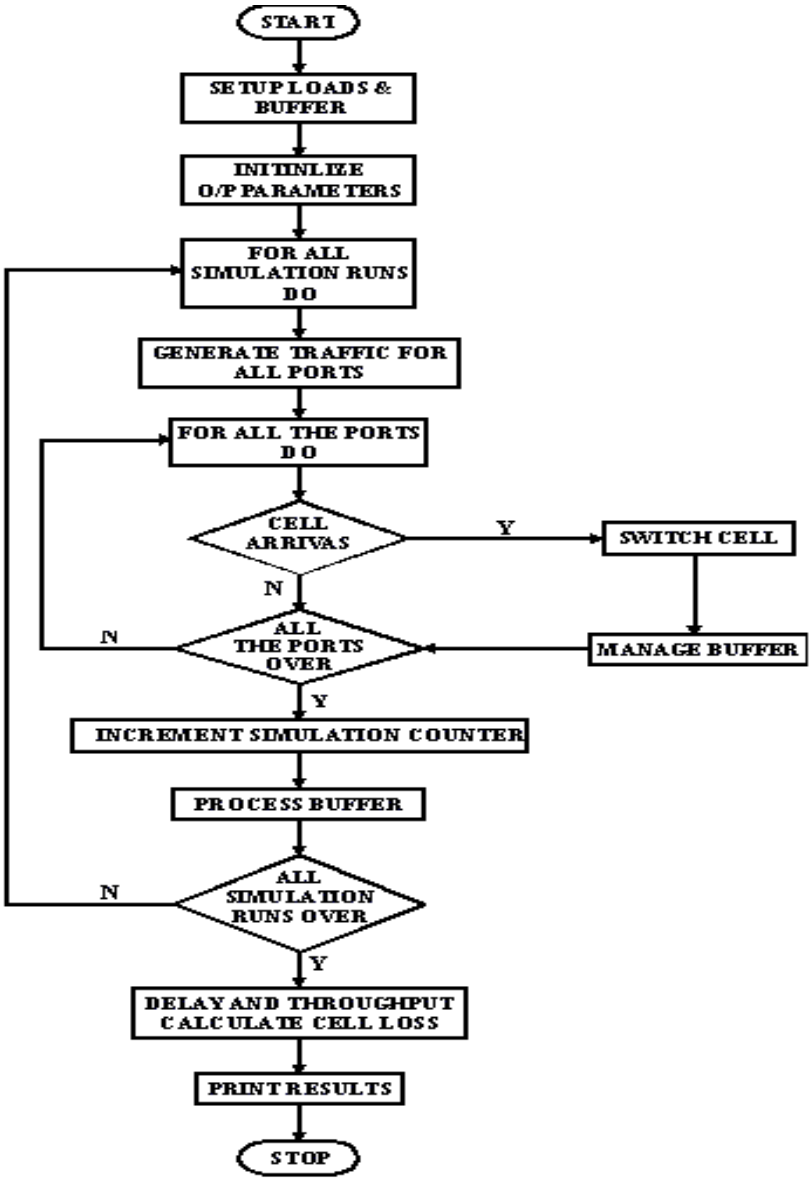

Fig. 6 - Flow Chart for Simulation Process

6.3 Initialize Parameters

All the out put parameters i.e. cell loss, unicast and multicast cell delay and throughput are initialized for all the ports and all simulation runs.

6.4 Initialize Sources and Buffer

All the VBR sources are initialized. For VBR sources, ON/OFF state are taken according to load and random number generator. The buffers are also initialized. At each input port for each time slot do the following.

Switching the Cells Arriving:

All the cells arriving at the input port are switched to corresponding output buffer for unicast cells.

- For multicast cells duplication is done (not in all the cases) before forwarding to destinations. If there is no cell, wait till next time slot.

Manage Buffer:

- If there is any cell in the output register of switching network, place it in buffer. If buffer is full, the cell will be lost. If buffer is not full, then apply various threshold schemes i.e. ST, DT, and proposed Fuzzy Threshold scheme as shown in Fig. 7(a), (b), and (c) respectively.

Increment Delay:

- The minimum service time is one slot-time, so after each slot, number of simulation time slot counter is increasing by one. Hence delay is automatically increase by one for all the cells (delay = simulation counter-cell generation time).

Process Buffer:

- At the end of each time slot, a cell is taken from each buffer and put into the sink for calculating the performance parameters and then free and number of cells field for buffer is updated.

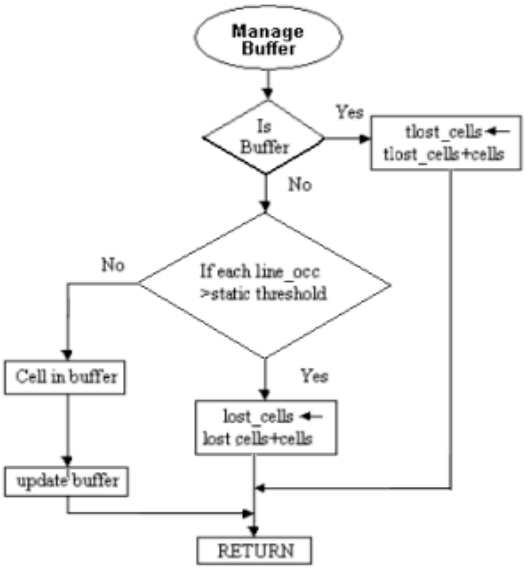

Fig. 7(a) - Flow Chart for Manage Buffer of Static Threshold Scheme

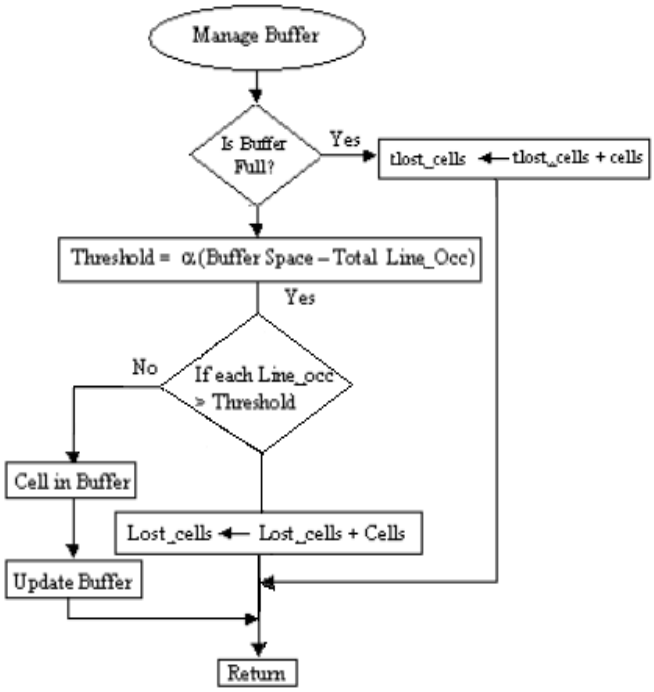

Fig. 7(b) - Flow-Chart for Manage Buffer of Dynamic Threshold Scheme

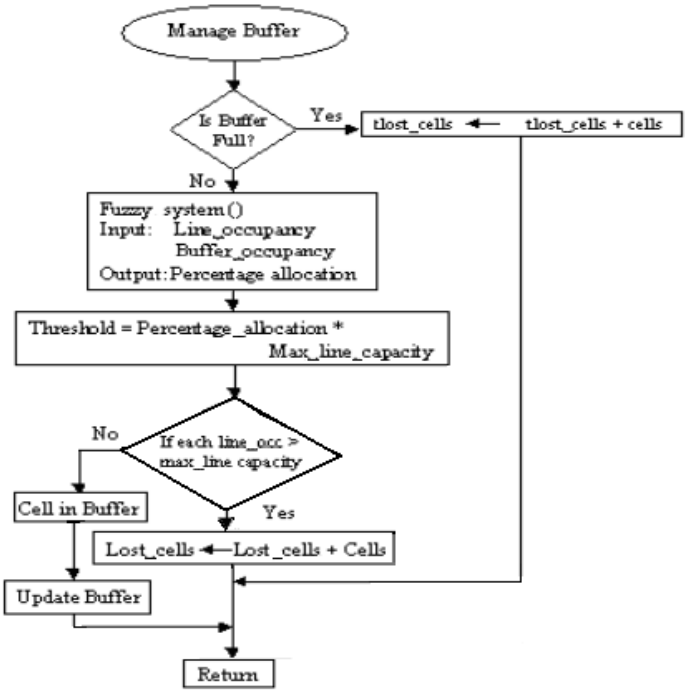

Fig. 7(c) - Flow-Chart for Manage Buffer of Fuzzy Threshold Scheme

7 Results

For modeling of an ATM switch, discrete-time model is used. Switch is $N \times N$ ATM switch, which uses output queueing and shared memory, i.e., each output port of the fabric has a logical queue, but these queues all share the same fabric memory. Time axis is slotted with slot size equal to a cell transmission time on the output link. In onetime slot, only one cell can be switched and other cells are put in input queue.

Cells arrivals and transmission are considered to occur at slot boundaries. Hence the minimum time required to serve a cell is one time slot. The standardized ATM cell size of 53 bytes leads to a transmission time 2.827 μs, at a transmission rate of 155.5 Mbps. The switch fabric randomly selects a maximum of $1 \le L \le N$ cells with the same output address and places them at their output buffer in one slot. A cell leaves its queue after receiving service of one time slot duration. Cells are served according to FIFO strategy. A cell arriving at a queue, which is full will be lost.

We first consider a nominal switch configuration with dimensions 64×64, buffer size (B) = 2048 cells.

Simulation results are taken for three burst lengths i.e. for BL = 20, BL = 30 and BL = 40. We compared the performance of proposed Fuzzy Threshold Scheme with Static Threshold (S.T.), Dynamic Threshold (D.T.) schemes. We have used Lookup Table 1(a) for rule based inference process, and Set I of Table 2 for Defuzzification purpose in our fuzzy scheme.

The performance of switch also evaluated when the multicast bursty traffic is under Without Threshold (W.T.). The value of constant Static Threshold is taken equal to 30, like Static Threshold the Dynamic Threshold has a single parameter, i.e., proportionality constant $\propto$. We have taken two values for this constant in our simulation i.e. $\alpha = 1.015625$ for D.T.(1) and $\alpha = 2.015625$ for D.T.(2).

In present work VBR traffic is used for the purpose. Each input VBR source i, $i = 1, 2, ..., N$, is modeled by two state ON-OFF Interrupted Bernoulli Process (IBP). The simulation results obtained for evaluation the performance of various congestion control schemes under unicast (90%) and multicast (10%) mixed traffic load are chosen as follows and presented in the form of Figs. 8 – 19.

- Average cell delay as experienced by unicast cells in the incoming mixed traffic
- Average cell delay as experienced by multicast cells in the incoming mixed traffic
- Average Throughput
- Cell Loss Rate

From the results we observed that all the QoS parameters as described above are the function of burst length and offered load. It has been shown from the Figs. 8-13, that for proposed Fuzzy Threshold scheme, average unicast as well as multicast cell delay for a given burst length is minimum under different load conditions.

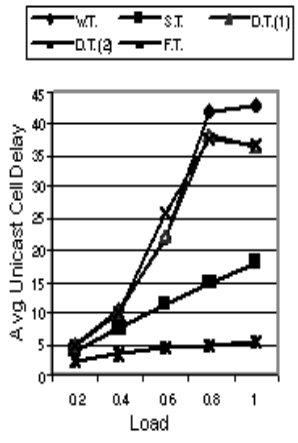

Fig. 8 - Average Unicast Cell Delay Vs Load, for BL=20

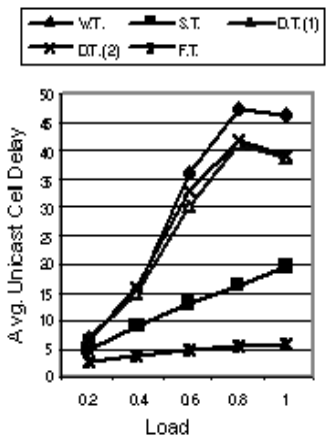

Fig. 9 - Average Unicast Cell Delay Vs Load, for BL=30

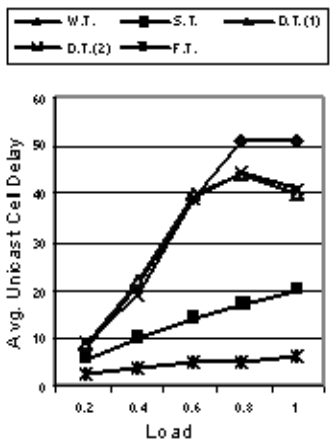

Fig.10 - Average Unicast Cell Delay Vs Load, for BL=40

The ST scheme shows the better performance in comparison to DT scheme for delay parameter. The reason for increase in average cell delay for unicast and multicast cells under DT scheme, the shared memory space is utilized more efficiently than that under ST scheme; and, as a result of efficient memory utilization, more cells are able to stay for a longer duration within the memory without being lost.

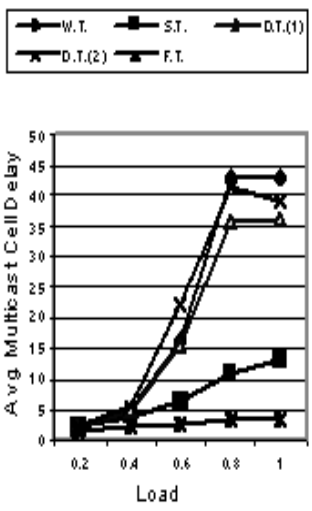

Fig.11 - Average Multicast Cell Delay Vs Load, for BL=20

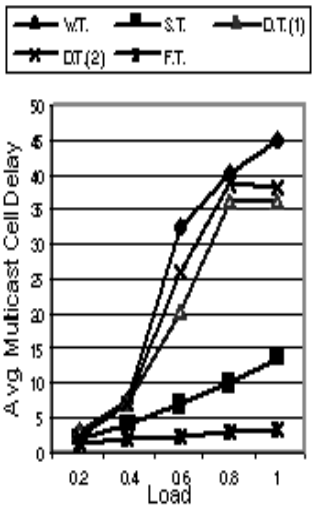

Fig. 12 - Average Multicast Cell Delay Vs Load, for BL=30

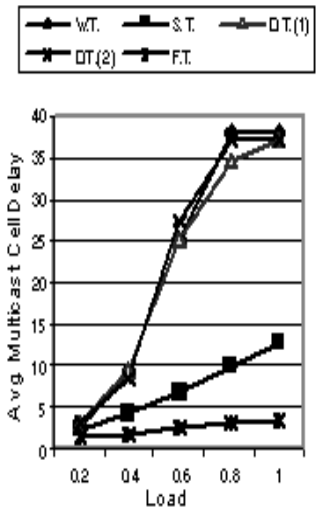

Fig. 13 - Average Multicast Cell Delay Vs Load, for BL=40

This phenomena decreases the cell loss rate at the cost of increasing the average queuing delay. The average unicast as well as multicast cell delay is maximum when there is no threshold applied on the incoming mixed bursty traffic.

From Figs. 14–16, we observed that, at the initial stage of the offered load (20% – 40%) all the schemes provide same throughput. Which shows that the switch serves all the incoming cells.

In a similar way when offered load increases from 40% to 60%, all the schemes show almost same behavior with a little difference in throughput. But at the higher loads (70% - 100%) the throughput for proposed Fuzzy Scheme is minimum, and it is maximum for DT Scheme.

The problem relates to the fact that the memory of the switch fabric is shared across all the ports or lines of that switching element.

Under most circumstances, this sharing is good for performance. There is a risk, however, that a small number of queues could become overloaded, take over all the shared memory in their switching element, and thereby block traffic to other queues.

It is indicated from Figs. 17–19 that average cell loss rate is minimum for DT threshold. As stated previously this is achieved at the cost of increasing in average cell delay. The second reason is that, the DT deliberately wastes a small amount of buffer space. This 'wasted' buffer space actually serves useful functions. The first advantage of maintaining some spare space all time is that this provides a cushion during transient periods when all output queue first become active. This reduces cell loss for newly active queue during such transients.

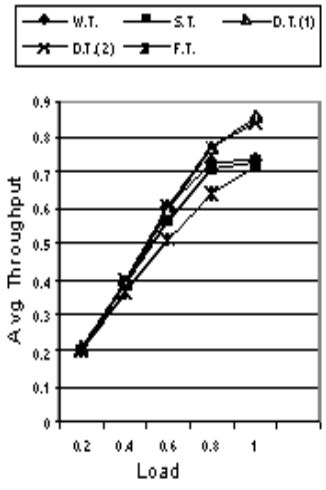

Fig. 14 - Average Throughput Vs Load, for BL=20

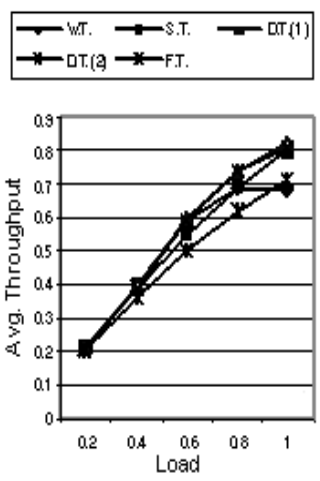

Fig. 15 - Average Throughput Vs Load, for BL=30

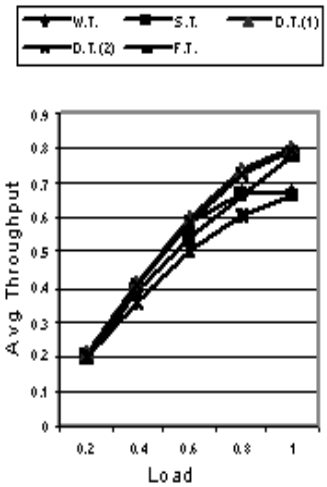

Fig. 16 - Average Throughput Vs Load, for BL=40

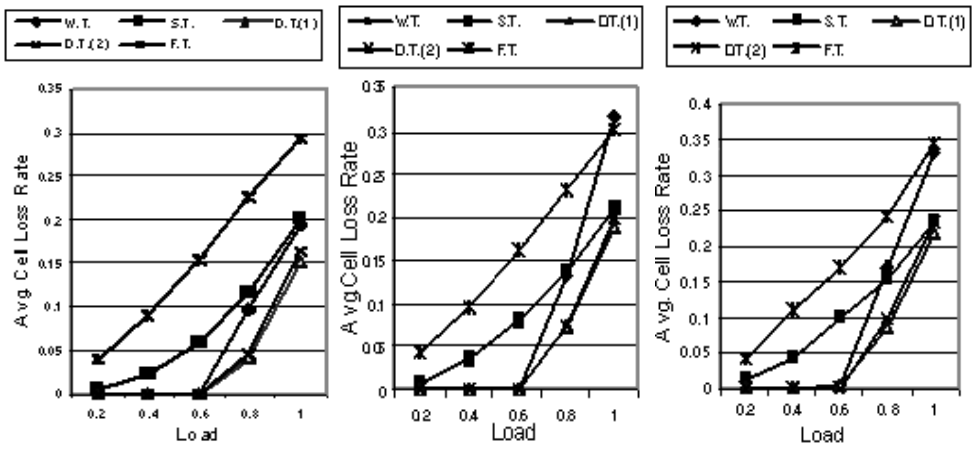

Fig. 17 - Average Cell Loss Rate Vs Load, for BL=20

Fig. 18 - Average Cell Loss Rate Vs Load, for BL=30

Fig. 19 - Average Cell Loss Rate Vs Load, for BL=40

8 Conclusions

In shared-memory ATM switches, queue length threshold/control can promote fair and efficient use of the packet buffer memory. The simplest control, Static Threshold (ST), works well as long as the threshold is tuned properly for the load condition. However, the ST is not robust to many sorts of load changes unless the threshold setting is retuned. To get good performance, one has to be especially careful not to set the threshold too low or too high. The attraction of ST is its ease of implementation. The results of the performance evaluations indicated that the throughput of the shared-memory switch improved when Dynamic Threshold (*DT*) is applied.

As stated earlier the reason behind this is that, memory space is utilized more efficiently in this scheme. So cells are able to stay for a longer duration within the memory without being lost. Naturally it reduces cell loss rate or increases throughput. Secondly, deliberately wasted buffer space by the scheme also reduces cell loss rate for newly active queue during transient's periods. DT is nearly as simple to implement as ST and, DT is adaptive.

At last, proposed fuzzy logic based scheme in which we consider two fuzzy variables namely line occupancy and buffer occupancy, according to fuzzification and defuzzification, we find the allocation space for each line queue up-to max-line capacity in shared memory switch, it means it is dynamically for every entering cell in ATM switch.

We used the Lookup-Tables 1(a) and 1(b) for fuzzification, and Sets of Table 2 for defuzzification, and find the trade-offs between average cell delay (unicast and multicast both) and throughput. Different Lookup-Tables based on experience and

different defuzzification sets can be used, so that parameters can get fine tuned to achieve a desired performance.

Finally the RAR scheme, which is used for multicast support for shared memory ATM switch, has its limitations and shortcomings, which are to be overcome. One of its demerits is inefficient memory utilization, as a result at higher load conditions cell loss rate becomes high.

Acknowledgment

The financial support from the University Grants Commission - New Delhi, under grant-in-aid-No. F-14-40/2000(S-I) is gratefully acknowledged. Authors would also like to thank the anonymous referees of this paper for valuable feedback that has considerably improved the presentation of this paper.

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